Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A system for arbitrating access to a shared resource comprising:

a plurality of microprocessors;

a shared resource; and

a controller coupled to the plurality of microprocessors and the shared resource by a first bus and a second bus, respectively, the controller including a register having a lock portion associated with each of the plurality of processors and ~~at least one~~ a status portion, each of the lock portions indicating whether the associated one of the plurality of microprocessors has obtained access to communicate with the shared resource, and ~~each of the at least one~~ the status portion[[s]] includes a bit indicating whether any of the plurality of microprocessors has obtained access to communicate with the shared resource.

2. (Previously presented) The system of claim 1 wherein the shared resource comprises a memory device.

3. (Previously presented) The system of claim 1 including a plurality of shared resources.

4. (Previously presented) The system of claim 3 wherein the register includes at least as many lock portions and status portions as there are shared resources, wherein each shared resource has a lock portion and a status portion associated therewith.

5. (Previously presented) The system of claim 1 wherein each of the lock portions comprises an arbiter device which accepts lock bits input from each of the plurality of processors and outputs the lock bit of a processor that addresses the arbiter device.

6. (Previously presented) The system of claim 5 wherein, when a particular processor requires access to the shared resource, it inputs a lock bit to the arbiter device.

7. (Previously presented) The system of claim 6 wherein, if no processor other than the particular processor has input a lock bit to the arbiter device, the arbiter device accepts the lock bit from the particular processor and enables the particular processor to access the shared resource.

8. (Previously presented) The system of claim 7 wherein, when access to the shared resources is enabled, a status bit in the status slice associated with the shared resource is set.

9. (Previously presented) The system of claim 6 wherein, if a processor other than the particular processor has previously input a lock bit to the arbiter device, the arbiter device clears the lock bit from the particular processor to zero.

10. (Previously presented) The system of claim 9 wherein, when access to the shared resources is enabled, a status bit in the status portion associated with the shared resource is set.

11. (Previously presented) The system of claim 8 wherein, after the particular processor inputs its lock bit to the arbiter device, the particular processor addresses the arbiter device to read its lock bit from the output of the arbiter device and reads the status bit associated with the shared resource.

12. (Previously presented) The system of claim 10 wherein, after the particular processor inputs its lock bit to the arbiter device, the particular processor addresses the arbiter device to read its lock bit from the output of the arbiter device and reads the status bit associated with the shared resource.

13. (Previously presented) A controller for arbitrating access to at least one shared resource by a plurality of processors, the controller comprising:

a first register portion including a plurality of layers, each of the plurality of layers being associated with a different one of the plurality of processors, each of the plurality of layers including an access indication portion associated with each of the at least one shared resource, the access indication portion holding an indicator of whether a processor associated with a particular layer has obtained access to communicate with the shared resource associated with the access indication portion of the particular layer; and

an access arbitration device associated with all of the access indication portions of each of the at least one shared resources for controlling access to the associated shared resource by the plurality of processors, the access arbitration device including an input for receiving access indication signals from the plurality of processors, the access arbitration device:

(A) determining whether the at least one shared resource is being accessed by any of the plurality of processors; and

(B) arbitrating access to the shared resource based on the determination made in Step (A).

14. (Previously presented) The controller of claim 13 wherein, if a particular processor of the plurality of processors requires access to a particular one of the at least one shared resources, it inputs an access indicator to the input of the access arbitration device associated with the particular shared resource and, if no other processor has access to the shared resource, as determined in Step (A), the access arbitration device grants access to the particular shared resource by the particular processor.

15. (Previously presented) The controller of claim 13 wherein, if a particular processor of the plurality of processors requires access to a particular one of the at least one shared resources, it inputs an access indicator to the input of the access arbitration device associated with the particular shared resource and, if another processor has access to the shared resource, as determined in Step (A), the access arbitration device denies access to the particular shared resource by the particular processor.

16. (Previously presented)The controller of claim 14 wherein the access arbitration device grants access to the particular shared resource by the particular processor by passing the access indicator input to the access arbitration device by the particular processor to the access indication portion for the particular shared resource in the layer associated with the particular processor.

17. (Previously presented)The controller of claim 15 wherein the access arbitration device denies access to the particular shared resource by the particular processor by clearing the access indicator input to the access arbitration device by the particular processor.

18. (Previously presented) The controller of claim 13 wherein the access arbitration device further includes a first logic device that performs Step (A) by receiving as inputs the contents of the access indication portions in all of the layers associated with the particular shared resource and outputting a signal in a first state if the shared resource is being accessed by one of the plurality of processors and in a second state if the shared resource is not being accessed by any of the plurality of processors.

19. (Previously presented) The controller of claim 18 wherein the access arbitration device further includes a second logic device that performs Step (B) by receiving the signal output by the first logic device and access indicator signals from the plurality of processors and outputting a signal of the first state when the output of the first

logic device is of the first state and a signal of the second state when the output of the first logic device is of the second state.

20. (Previously presented) The controller of claim 19 wherein the first logic device includes an OR gate having its output inverted.

21. (Previously presented) The controller of claim 20 wherein the second logic device includes an AND gate.

22. (Previously presented) The controller of claim 19 wherein the access arbitration device further comprises a write device that receives the signal output by the second logic device as an input and writes its input to the access indication portion of the processor that sent the access indication signal to the access arbitration device, the write device being instructed as to which access indication portion to output its input by a select signal input to the write device by the processor that sent the access indication signal to the access arbitration device.

23. (Previously presented) The controller of claim 13 wherein the access arbitration device further comprises a read device which receives as inputs the contents of the access indication portions in all of the layers associated with the particular shared resource and reads out the contents of one of the access indication portions, the read device being instructed as to which access indication portion to read out by a read select signal input to the read device by a processor that inquires as to the contents of the access indication portion associated with the processor.

24. (Previously presented) The controller of claim 23 wherein the access arbitration device further comprises a read device which receives as inputs the contents of the access indication portions in all of the layers associated with the particular shared resource and reads out the contents of one of the access indication portions, the read device being instructed as to which access indication portion to read out by a read select

signal input to the read device by a processor that inquires as to the contents of the access indication portion associated with the processor.

25. (Previously presented) The controller of claim 13 further comprising a second register portion including a status indication portion associated with each of the at least one shared resources, each status indication portion including a status indicator which indicates whether the shared resource associated with the status indication portion is being accessed by one of the plurality of processors.

26. (Previously presented) The controller of claim 24 further comprising a second register portion including a status indication portion associated with each of the at least one shared resources, each status indication portion including a status indicator which indicates whether the shared resource associated with the status indication portion is being accessed by one of the plurality of processors.

27. (Previously presented) The controller of claim 26 wherein, in order to determine the status of a particular one of the at least one shared resources, a processor reads the status indication portion of the particular shared resource to determine whether the particular shared resource is being accessed and inputs a read select signal to the read device to instruct the read device to read out the contents of the access indication portion associated with the processor to determine whether it has access to the particular shared resource.

28. (Currently amended) A method of arbitrating access to a shared resource by a plurality of processors, the method comprising:

A) processing access indication signals received from each of the plurality of processors;

B) storing the processed access indication signals;

C) performing a logic operation on the processed access indication signals to generate an access arbitration signal;

D) receiving [[an]] a further access indication signal from a particular one of the plurality of processors; and

E) arbitrating access to the shared resource by the particular processor based on the state of the access arbitration signal.

29. (Previously presented) The method of claim 28 wherein Step E further comprises granting access to the shared resource by the particular processor if the access arbitration signal is of a first state.

30. (Previously presented) The method of claim 29 wherein Step E further comprises blocking access to the shared resource by the particular processor if the access arbitration signal is of a second state.

31. (Previously presented) The method of claim 30 further comprising:

F) outputting a stored processed access indication signal for the particular processor when instructed by the particular processor, wherein the stored processed access indication signal for the particular processor indicates whether the particular processor has access to the shared resource.